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A Quad Coding Technique to Reduce Transition Activity in VLSI Circuits

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Abstract—*Advances in VLSI technology have enabled the implementation of complex circuits in a single chip, reducing power consumption. System on chip design in submicron techniques interconnect plays an important role in overall performance of chip. The main cause of energy dissipation is charging and discharging of internal node capacitance due to transition activity, when an input signal changes, energy transition occurs, which causes to charge or discharge capacitive load of cmos circuit which induces power dissipation.*

There are several methods for reducing power dissipation; among them a quad coding method is effective. The key aspect of this method is to reduce power dissipation by minimizing transition activity which is achieved by introducing various data coding schemes.

This coding technique is implemented in this paper using verilog HDL and analyzed by using Xilinx ISE simulator 14.2.

1. INTRODUCTION

Energy consumption is one of the major aspects in the design of VLSI circuits. As the technology scales down to deep submicron technology the bus energy reduction has become more and more important. In order to optimize the power dissipation of digital systems low power methodology should be applied throughout the design process from system level to process level.

With the increase in speed, mobility and miniaturization of current electronic products power consumption has become major design factor, especially for hand held devices, the power consumption determines the battery life time. Therefore, the designers and consumers of electronic devices as well as environmental considerations demand a reduction in power dissipation of digital circuits. Thus the parts or blocks consuming an important fraction of the power are properly optimized for power saving.

So all the researchers worked on reducing transition activity on buses using Bus invert coding, shift invert coding rotate coding, and coding for energy reduction in VLSI interconnects Here one or two coding techniques are used to reduce the transition activity. In this paper we introduce a quad coding technology to reduce the transition activity and an energy estimator block is implemented by using CMOS logic to minimize the device count. Here the random data are coded in 4 different ways to reduce the transition activity. This design will give better power saving performance than other existing methods.

The rest of the paper is organized as follows: Definitions of some of the important terms are used in this paper are given in section II Bus Energy Model given in section III Power dissipation is given in section IV and a brief overview of the related bus coding is given in section V. The proposed coding scheme is explained in section VI while Simulation and Results of proposed coding scheme with an example is shown in section VII, Finally conclusions are made in section VIII.

2. SOME RELATED TERMS.

1) **Transition activity:** This is defined as due to charging and discharging, the data changed from 1 to 0 or from 0 to 1 between adjacent bus wires or on the same bus wire.

(1) Transition between adjacent bus wires is called coupling transition;

(2) Transition between neighboring data on the same bus wire is called self transition.

2) **Hamming distance**: The Hamming distance between the two code vectors is equal to the number of elements in which they differ.

Example:

Let Y = 11110000

Let X = 11001100

Here only four bits differ from each other between X and Y,

Hence Hd (X,Y) = 4

3. TYPES OF POWER DISSIPATION

To minimize the power consumption of a CMOS circuit the various power components and their effects must be identified. Power dissipation is the most critical parameter for portability

and mobility and it is classified into dynamic and static power dissipation

4. SOURCES OF POWER DISSIPATION.

These are major sources of power dissipation in digital CMOS circuits. They are.

1) Static power

2) Dynamic power

Static power caused by the leakage current I_{leak} and other static component I_{st} due to the value of the input voltage.

Dynamic power is caused by the total output capacitance C_L and by the short circuit current I_{sc}, during the switching transients.

The total power dissipation can be obtained from the sum of the dissipation components:

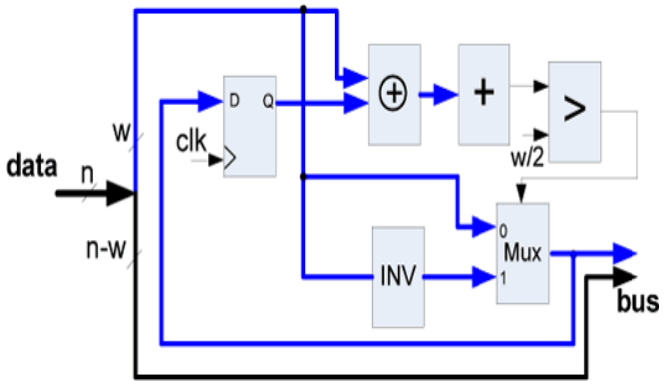
$P_{tot} = P_{dynamic} + P_{short\text{-}circuit} + P_{Leakage}$.

Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in a power-down mode. The static power dissipated by a CMOS VLSI is in the Nano watt range. So we consider dynamic power issues in this paper. Because dynamic power dissipation is the most dominant component, its contribution ranges between 70% to 80% of the total power consumption, thus we focus on methods that estimate the dynamic power consumption.

5. VARIOUS TYPES OF CODING SCHEMES.

1) Bus Invert Coding.

This method uses an extra control bit called an invert. The Hamming distance (the number of transitions) between the present bus value and the next data value is computed. If this Hamming distance is greater than n/2, where n is the width of the bus, then the data value is inverted (bit complemented) and transmitted over the bus. In this case invert bit equals to 1. If the Hamming distance is not greater than n/2, then the data value is transmitted as it is. In this case invert bit equals to 0..



2) Partial bus-invert coding.

In PBI coding, we partition a bus into two sub buses based on the behavior of patterns transferred. For example, partition a bus B into a selected sub bus S and the remaining sub bus R such that S contains bus lines having higher transition correlation and/or higher transition probability and R contains the remaining bus lines. Because the bus lines in R have low correlation with those in S and low transition activity, inverting those in R may increase rather than decrease the transition activity. Therefore, by applying BI coding only to the sub bus S, we can reduce the hardware overhead as well as decrease the total number of bus transitions.

3) Shift-Inv technique.

In this technique we shift the data bits by one bit position (left-shift and right-shift) if the shifting reduces the number of transitions. Among four operations, namely, data shifted left, shifted right, inverted and sent as unmodified, whichever gives the least number of transitions that data is sent on the bus. To indicate the operation performed it requires two extra bits.

6. PROPOSED CODING SCHEME

Power Model

The dynamic power consumed by the interconnects and drivers is given by

$$P = [T_{0\to1}(C_s + C_l) + T_c C_c]\, V_{dd}^2 F_{ck}$$

where V_{dd} is the supply voltage, F_{ck} is the clock frequency, C_s is the self capacitance (which includes the parallel-plate capacitance and the fringe capacitance), C_l is the load capacitance, and C_c is the coupling capacitance. $T_{0\to1}$ and T_c are the average number of effective transitions per cycle for C_s and C_c, respectively. They are computed as follows. $T_{0\to1}$ counts the number of $0 \to 1$ transitions in the bus in two consecutive transmissions. T_c counts the correlated switching between physically adjacent lines. Also $T_{0\to1}$ represents the transition activity over a bus in which transition takes place from 0 to 1,it is also called as self switching activity. Tc represents the coupling switching activity over adjacent buses. Dynamic power largely depends on these two switching activities. While the other parameters are assumed to be constant (as their variations are small) thereby reducing T0→1 and Tc, dynamic power is greatly reduced.

Let X be the n bit wide data present on the bus at time instant k is defined as $X = (xk_{n-1}, xk_{n-2}, \ldots xk_1, xk_2)$.. Let Y be the Reference data transmitted on the bus. Let d be the hamming distance between the buses. M_d is the minimum hamming distance between the coded data and reference data. Here input data has been chosen randomly and coded in four different ways such as rotate left invert, rotate right invert, circular left shift, circular right shift combining all in a single suite named as quad Coding technique to code a 8 bit random

data sample. Hamming distance d is calculated for all the coding techniques. With respect to the minimum hamming distance, one coding technique is selected and another discarded. The four coding methods are as:

1) Rotate Left Invert

2) Rotate Right Invert

3) Circular Left Shift

4) Circular Right Shift

Rotate Left Invert: In this method the current bits are rotated left by one bit and then the bits are inverted.

Rotate Right Invert: In this method the current bits are rotated right by one bit and then the bits are inverted.

Circular Left Shift: In this method the current bits are circularly rotated left by one bit.

Circular Right Shift: In this method the current bits are circularly rotated left by one bit.

S. NO	CODING METHOD	CONTROL BIT
1	Rotate Left Invert	00
2	Rotate Right Invert	01
3	Circular Left Shift	10
4	Circular Right Shift	11

We have grouped the above four techniques into two groups, namely group 1 and group 2.

Group 1

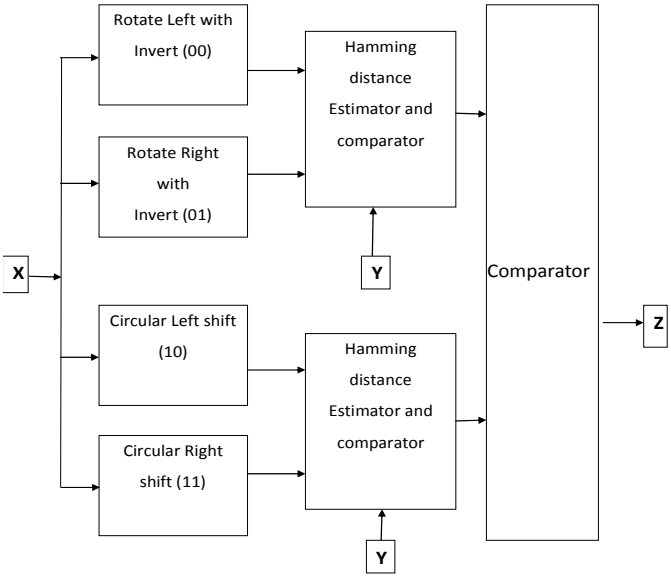
This group consists of two coding methods named invert rotate left with invert/rotate right with invert. Rotate left by one bit of X then invert and append a control bit. The new data is defined as 'rli' .Rotate right by one bit of X and append a control bit. The new data is defined as 'rri'.

Group 2

This group consists of two coding methods named circular left shift/circular right shift. Shift left the bits of X circularly and append a control bit. The new data is defined as 'cls'. Shift right the data bits of X circularly and append a control bit. The new data is defined as 'crs'.

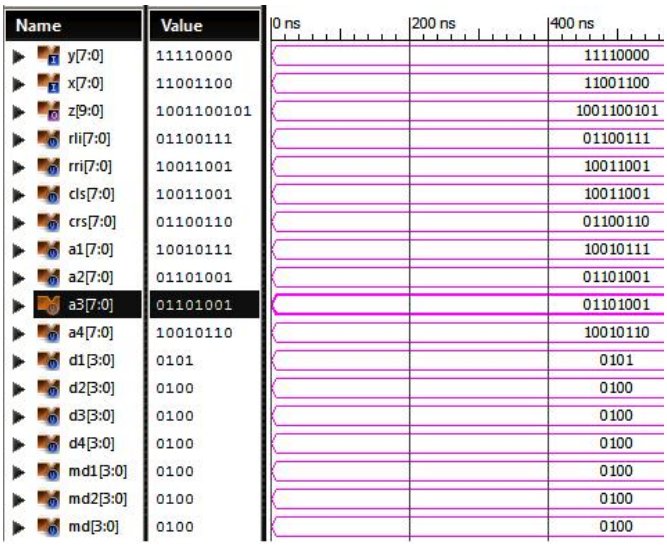
Hamming distance M_d (group1, group 2) is calculated and the group having minimum hamming distance is transmitted.

7. HARDWARE IMPLEMENTATION



8. SIMULATION RESULTS

The Hardware model is simulated using a Verilog Xilinx Isim simulator. Output is verified using 8 bit random sample X=11001100 and the previous value Y=11110000.



9. CONCLUSION

A simple approach is proposed in this paper to reduce the transition activity and power. In a quad coding technique 8 bit random data is coded in four possible ways to reduce the number of transition activity. This proposed technique is more effective in reducing power consumption. The result is simulated using ISE Design Suite 14.2 software and the power calculations are carried out using Xpower Analyzer (XPA) inbuilt tool of ISE.The simulation result shows the overall reduction upto 31% as compared to the previous methods.

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